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UNITED STATES DISTRICT COURT
DISTRICT OF MASSACHUSETTS

ACQIS, LLC, Plaintiff, v. EMC CORPORATION, Defendant.	C.A. No. 1:14-cv-13560-ADB

DEFENDANT EMC CORPORATION'S OPENING CLAIM CONSTRUCTION BRIEF

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TABLE OF ABBREVIATIONS

Abbreviation	Document(s)
'119 patent	U.S. Patent No. RE43,119 (issued Jan. 17, 2012) (D.I. 32-10)
'171 patent	U.S. Patent No. RE43,171 (issued Feb. 7, 2012) (D.I. 32-7)
'185 patent	U.S. Patent No. 6,216,185 (issued Apr. 10, 2001) (related to the asserted patents)
'185 Reexam, Resp. to OA	Patent Owner's Response to Final Office Action in the reexamination of the '185 patent (May 3, 2011) (Ex. 17)
'294 patent	U.S. Patent No. RE41,294 (issued Apr. 27, 2010) (D.I. 32-5)
'416 patent	U.S. Patent No. 7,363,416 (issued Apr. 22, 2008) (D.I. 32-1)
'468 patent	U.S. Patent No. RE44,468 (issued Aug. 27, 2013) (D.I. 32-8)
'487 patent	U.S. Patent No. 7,818,487 (issued Oct. 19, 2010) (D.I. 32-3)
'624 patent	U.S. Patent No. 7,676,624 (issued Mar. 9, 2010) (D.I. 32-2)
'779 patent	U.S. Patent No. 7,376,779 (issued May 20, 2008) (related to the asserted patents)
'779 Reexam, Decision on Appeal	Decision on Appeal to the Patent Trial and Appeal Board in the reexamination of the '779 patent (Oct. 28, 2013) (Ex. 18)
'814 IPR	IPR2014-01469 (challenging the '814 patent)
'814 IPR Decision	Final Written Decision, IPR2014-01469 (Mar. 8, 2016) (D.I. 126-5)
'814 IPR Inst.	Decision, Institution of *Inter Partes* Review, IPR2014-01469 (Mar. 11, 2015) (D.I. 126-3)
'814 patent	U.S. Patent No. RE42,814 (issued Oct. 4, 2011) (D.I. 32-6)
'873 IPR	IPR2014-01462 (challenging the '873 patent)
'873 IPR Decision	Final Written Decision, IPR2014-01462 (Mar. 8, 2016) (D.I. 126-4)
'873 IPR Inst.	Decision, Institution of *Inter Partes* Review, IPR2014-01462 (Mar. 11, 2015) (D.I. 126-2)
'873 patent	U.S. Patent No. 8,041,873 (issued Oct. 18, 2011) (D.I. 32-4)
'961 patent	U.S. Patent No. RE41,961 (issued Nov. 23, 2010) (D.I. 32-11)
'984 patent	U.S. Patent No. RE42,984 (issued Nov. 29, 2011) (D.I. 32-9)
ACQIS '814 IPR Prelim. Resp.	Patent Owner's Preliminary Response, IPR2014-01469 (Dec. 15, 2014) (Ex. 3)
ACQIS '814 IPR Resp.	Patent Owner's Response, IPR2014-01469 (June 11, 2015) (Ex. 5)

Abbreviation	Document(s)
ACQIS '814 IPR Surreply	Patent Owner's Surreply, IPR2014-01469 (Nov. 6, 2015) (Ex. 11)
ACQIS '873 IPR Prelim. Resp.	Patent Owner's Preliminary Response, IPR2014-01462 (Dec. 15, 2014) (Ex. 2)
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ACQIS EDTX Opening CC Br.	Plaintiff ACQIS LLC's P.R. 4-5(a) Opening Claim Construction Brief, D.I. 129, *ACQIS LLC v. Alcatel-Lucent USA Inc. et al.*, No. 6:13-cv-638 (E.D. Tex. Jan. 5, 2015)
Board	Patent Trial and Appeal Board
Bogaerts	A. Bogaerts et al., *RD24 Status Report: Application of the Scalable Coherent Interface to Data Acquisition at LHC* (Oct. 1996) (at issue in the IPR of the '814 patent) (Ex. 16)
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Decl.	Declaration
Dominguez Decl.[1]	Declaration of Katherine Dominguez in Support of EMC's Opening Claim Construction Brief, submitted concurrently herewith
EMC '814 IPR Reply	Petitioner's Reply, IPR2014-01469 (Sept. 10, 2015) (Ex. 8)
EMC '873 IPR Reply	Petitioner's Reply, IPR2014-01462 (Sept. 10, 2015) (Ex. 7)
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Fig.	Figure
Horst	Robert W. Horst, *TNet: A Reliable System Area Network* (Feb. 1995) (at issue in the IPRs of both the '814 and '873 patents) (Ex. 15)
IBM 2-14 Trial Tr.	Trial transcript from Feb. 14, 2011, D.I. 687, *ACQIS, LLC v. Appro Int'l, et al.*, No. 6:09-cv-148 (Ex. 19)
IBM 2-15 Trial Tr.	Trial transcript from Feb. 15, 2011, D.I. 689, *ACQIS, LLC v. Appro Int'l, et al.*, No. 6:09-cv-148 (Ex. 20)

[1] Citations in this brief to "Ex. X" are citations to the exhibits attached to the Dominguez Decl., unless otherwise noted.

Abbreviation	Document(s)
IPR	*inter partes* review
IPR Hr'g Tr.	Transcript of Oral Hearing before the Patent Trial and Appeal Board, IPR2014-01462, -01469 (Dec. 8, 2015) (Ex. 13)
Lindenstruth Decl.	Declaration of Volker Lindenstruth (ACQIS technical expert) filed by ACQIS in IPR2014-01469 (June 10, 2015) (Ex. 6)
Lindenstruth Dep. Tr.	Deposition transcript of Volker Lindenstruth (ACQIS technical expert) in IPR2014-01462 and IPR2014-01469 (Aug. 27-28, 2015) (Exs. 9–10)
PCI	Peripheral Component Interconnect
PCI standard	PCI Local Bus Specification, Revision 2.1 (June 1, 1995) (Ex. 14)
PTO	United States Patent and Trademark Office
Young Decl.	Declaration of Bruce Young (EMC technical expert) in Support of *Inter Partes* Review of U.S. Patent No. RE42,814 (Ex. 1)

TABLE OF EXHIBITS

Exhibit	Document
Exhibit 1	Excerpts of the Declaration of Bruce Young in Support of *Inter Partes* Review of U.S. Patent No. RE42,814 filed by EMC in IPR2014-01469 (Sept. 10, 2014).
Exhibit 2	Patent Owner's Preliminary Response filed by ACQIS in IPR2014-01462 (Dec. 15, 2014).
Exhibit 3	Patent Owner's Preliminary Response filed by ACQIS in IPR2014-01469 (Dec. 15, 2014).
Exhibit 4	Patent Owner's Response filed by ACQIS in IPR2014-01462 (June 11, 2015).
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Exhibit 6	Excerpts of the Declaration of Volker Lindenstruth filed by ACQIS in IPR2014-01469 (June 10, 2015).
Exhibit 7	Petitioner's Reply filed by EMC in IPR2014-01462 (Sept. 10, 2015).
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Exhibit 9	Excerpts of the transcript of deposition of Volker Lindenstruth in IPR2014-01462 and IPR2014-01469 (Aug. 27, 2015).
Exhibit 10	Excerpts of the transcript of deposition of Volker Lindenstruth in IPR2014-01462 and IPR2014-01469 (Aug. 28, 2015).
Exhibit 11	Patent Owner's Surreply, filed by ACQIS in IPR2014-01462 (Nov. 6, 2015).
Exhibit 12	Patent Owner's Surreply, filed by ACQIS in IPR2014-01469 (Nov. 6, 2015).
Exhibit 13	Excerpts of the transcript of Oral Hearing before the Patent Trial and Appeal Board, IPR2014-01462, -01469 (Dec. 8, 2015).
Exhibit 14	Excerpts of the PCI Local Bus Specification, Revision 2.1 (June 1, 1995).
Exhibit 15	Robert W. Horst, *TNet: A Reliable System Area Network* (Feb. 1995).
Exhibit 16	A. Bogaerts et al., *RD24 Status Report: Application of the Scalable Coherent Interface to Data Acquisition at LHC* (Oct. 1996).
Exhibit 17	Patent Owner's Response to Final Office Action, filed by ACQIS in the *ex parte* reexamination of U.S. Patent No. 6,216,185 (May 3, 2011).
Exhibit 18	Decision on Appeal in the *inter partes* reexamination of U.S. Patent No. 7,376,779 (Oct. 28, 2013).
Exhibit 19	Excerpts of Transcript of Trial Afternoon Session, D.I. 687, *ACQIS, LLC v. Appro Int'l, et al.*, No. 6:09-cv-148 (Feb. 14, 2011).
Exhibit 20	Excerpts of Transcript of Trial Afternoon Session, D.I. 689, *ACQIS, LLC v. Appro Int'l, et al.*, No. 6:09-cv-148 (Feb. 15, 2011).
Exhibit 21	ACQIS, LLC's Understanding of Claim Terms, *ACQIS, LLC v. EMC Corp.*, No. 1:14-cv-13560 (D. Mass. Dec. 15, 2016).

I. Introduction

Each of the three claim constructions EMC proposes is compelled by the plain language of the claims and uniform teachings of the patent specifications, as well as by the representations ACQIS made during the recent IPR proceedings. EMC confines this brief to three terms concerning which ACQIS made binding statements in the IPR that limit the scope of the claims.[2]

At the outset, in order to broaden its patent claims beyond all recognition, ACQIS proposes constructions that are utterly divorced from, and contrary to, the plain language of the claims and the entirety of the specifications. For the phrase "PCI bus transaction," for example, ACQIS actually proposes a construction that requires *neither* a "PCI bus" *nor* a "transaction."

Not only are ACQIS's proposed constructions contrary to the plain language of the claims, they also are wholly inconsistent with—and legally precluded by—binding statements ACQIS made during the IPRs to preserve the validity of its patents. In granting the stay, this Court recognized that the IPRs, regardless of outcome, were likely to simplify the issues and affect the scope of the claims by virtue of positions ACQIS would take. That is exactly what happened: to distinguish prior art, ACQIS made explicit, binding statements regarding the scope of the claims, repeatedly advocating for narrow constructions of key terms. In so doing, ACQIS not only succeeded in saving its patents from the validity challenge in the PTO, but also obtained the significant benefit of EMC being estopped regarding certain prior art arguments in this court. Having avoided invalidity in the IPRs, ACQIS is bound by its statements regarding the scope of

[2] EMC confines this briefing to these three issues in light of the discussion with the Court regarding the impact of the IPRs on this case. As EMC explained, ACQIS's representations concerning claim scope in the IPRs limit the scope of the claims in ways that directly affect infringement in this case, and EMC will address that promptly, including in summary judgment. Given the extent to which the constructions addressed herein are compelled by ACQIS's statements and will simplify this case, EMC does not address any other claim construction issues at this time. EMC reserves its rights to do so, and maintains its objections to Judge Davis's other constructions, and will address those terms as necessary in the future.

the claims; those statements are now part of the intrinsic record and limit the scope of the claims.

Incredibly, however, despite defeating the IPRs by urging narrow readings of its claims, ACQIS now asks this Court to adopt constructions totally at odds with its statements in the IPRs by blindly adopting the broader constructions Judge Davis entered before the IPRs. ACQIS's proposal is irreconcilable with, and would entirely defeat the purpose of, the stay—which recognized that statements ACQIS made in the IPRs limit the scope of the claims. ACQIS's proposal also is indefensible as a matter of law and fundamental fairness. ACQIS is improperly trying to define its claims one way (*i.e.*, narrowly) in the IPRs to avoid invalidity and a totally different way (*i.e.*, broadly) in this Court to prove infringement. Such an approach is the height of gamesmanship and legally untenable. ACQIS's statements in the IPRs (made long after Judge Davis's claim construction order) are now part of the intrinsic record and limit the scope of the claims in this case as a matter of law, as the Federal Circuit has repeatedly and unequivocally held. ACQIS's binding statements to the PTO compel the constructions EMC proposes here.

II. Background

ACQIS currently accuses EMC of infringing 22 claims across 11 patents. *See* Appendix A (setting forth each asserted claim). The patents fall into three inter-related families: (1) the '873 Family: '416, '624, '487, and '873 patents; (2) the '814 Family: '294, '814, '119, and '961 patents; and (3) the '468 Family: '171, '984, and '468 patents. These patents descend from related applications filed by the same inventor, and describe virtually identical subject matter.[3]

The patents are all directed to various aspects of a "modular" computer system, *i.e.*, a system in which different computing components can be readily inserted or removed from a "console" that houses them. The patents disclose a module with a CPU and memory that inserts

[3] *See* D.I. 102 at 7–8. EMC will cite to a representative patent from each family, specifically the '873, '814, and '468 patents.

into a console having all of the necessary peripheral devices (*e.g.*, monitor, keyboard, mouse, modem, etc.) "to form a functional computer." *See* '814 patent at 3:28–29, 6:19–34, 7:48–60; *see also* '873 patent at 9:41–10:16; '468 patent at 7:57–8:14. The benefit of this arrangement, according to the patents, is that a user can carry the same module to separate consoles (say, at home and at work), thus "provid[ing] reduced user investment in redundant computer components." '814 patent at 3:16–19.

ACQIS did not invent modular computing. Young Decl. (Ex. 1), ¶¶ 53, 102–103, 110; IBM 2-14 Trial Tr. (Ex. 19) at 133:10–136:14. ACQIS's invention was directed at a particular improvement on the *interface* between the existing modules and consoles, *i.e.*, an improvement in the way modules and consoles communicated with each other. *Id.* at 136:20–137:8. At the time of the invention in the late nineties, many computing devices, including existing modules and consoles, relied on a well-known industry standard architecture known as the "PCI bus" architecture. *See* IBM 2-15 Trial Tr. (Ex. 20) at 148:11–150:2; Lindenstruth Decl. (Ex. 6), ¶¶ 59–60, 79. The characteristics of a PCI bus and the requirements for communications on the bus are defined by the PCI Local Bus Specification ("PCI standard"). *See id.* ¶¶ 21, 59. The PCI standard is referenced in every patent, and is incorporated in every asserted claim. *See, e.g.*, '873 patent at 3:14; Appendix A; *see also* ACQIS '814 IPR Prelim. Resp. (Ex. 3) at 7–9; D.I. 71 at 6.

A PCI bus is a set of circuitry (*i.e.*, wires) inside a computing device (*e.g.*, module and/or console) that interconnects the different computing components together, and allows them to communicate with each other. Lindenstruth Decl. (Ex. 6), ¶¶ 43, 59–60. One aspect of the PCI standard is that signals sent over a PCI bus are sent in what is known as a "parallel" format. *Id.* ¶¶ 54, 59–60, 62. The format is referred to as "parallel" because the wires are next to each other, and data is sent down the parallel wires at the same time. *Id.*; Young Decl. (Ex. 1), ¶ 25.

ACQIS identified a perceived problem with using this existing parallel PCI architecture in a modular computer system. Because both modules and the consoles used PCI buses that transferred data in parallel format, prior art systems often used parallel interface connectors to connect these modules and consoles together. *See* '873 patent at 3:11-21. According to ACQIS, the parallel interface connectors had certain drawbacks, particularly in a modular computer system, as these connectors were costly, bulky, cumbersome to handle, and, ultimately, too slow. *See, e.g.*, *id.* at 3:32–67; '814 patent at 19:46–62; '468 patent at 17:31–47.

ACQIS knew that it had to work with the underlying parallel standard PCI architecture because it was prevalent in existing modules and consoles. According to ACQIS, because "PCI had been widely adopted" and the industry "would not easily abandon it," it was necessary to "develop[] a system to speed up PCI transactions that was completely compatible with existing peripheral devices." ACQIS '814 IPR Resp. (Ex. 5) at 3.

ACQIS's idea was to use the modules and consoles incorporating standard PCI hardware, but to use a smaller, faster *interface* between those modules and consoles. According to ACQIS, its solution was an interface that would take the PCI signal from its original parallel form and convert it into what is known as "serial" form, and send the signal down a serial (not parallel) connector. *See* ACQIS '814 IPR Resp. (Ex. 5) at 3–6. The format is referred to as "serial" because, unlike with the parallel format, data sent down the serial connector is not sent down all at once, but rather a piece at a time. *See* Lindenstruth Decl. (Ex. 6), ¶ 56. As ACQIS explained in the IPR: "one key to the invention was to serialize the otherwise parallel PCI bus transactions to increase communications speeds." ACQIS '814 IPR Resp. (Ex. 5) at 3. According to ACQIS, converting the parallel PCI signals into serial form and transmitting the serial signals over the serial connectors was advantageous because the connectors, with fewer conductive lines, were

generally faster than parallel connectors. '873 patent at 5:49–62; Lindenstruth Decl. (Ex. 6) ¶ 58.

Importantly, because the existing modules and consoles connected by ACQIS's new serial interface still themselves used the existing parallel PCI architecture, those modules and consoles still needed to receive parallel signals in accordance with the PCI standard. ACQIS '814 IPR Resp. (Ex. 5) at 2–3, 8–10. Accordingly, ACQIS explained that another key aspect of the claimed invention was that all of the data required by the PCI industry standard—that is, all of the data that had been in parallel form and then converted to serial—would have to be preserved during communication. *See id.*; *see also* IPR Hr'g Tr. (Ex. 13) at 31:18–32:4. In this way, the serial transmission could be converted back to fully compliant parallel PCI signals that would be understood at the receiving end, "so that the serialized communications were compatible with existing peripheral devices." ACQIS '814 IPR Resp. (Ex. 5) at 3, 10. Otherwise, these devices would simply not understand each other. *See id.*

In sum, ACQIS purported to provide a new interface that (1) connects modules and consoles that rely on prior art PCI architectures; (2) converts the parallel PCI signals they produce into serial form for transmission over a serial connector; and (3) preserves all data required by the PCI standard during the communication process. EMC's three proposed constructions properly capture these core aspects of the invention.

III. Legal Standards for Claim Construction

A. Claim Construction Orders Are Non-Final and Subject to Change Until Trial

In response to EMC's request that this Court construe certain disputed terms, ACQIS contends that "the claim terms EMC proposes have already been construed by the Court, and those constructions should not be disturbed." ACQIS CC Stmt. (Ex. 21) at 1. ACQIS is incorrect on both counts: *this* Court has not yet construed *any* claim terms, and there have been critical developments during the IPRs, after the prior court issued its claim construction order,

that require that certain claim constructions be adopted by this Court.

Even if one were to ignore the IPRs entirely, ACQIS would be wrong to suggest that the Eastern District of Texas *Markman* Order controls in this case. Judge Davis himself acknowledged that this Court "will not be bound by [his] *Markman* opinion." D.I. 44 at 12–13. In fact, pretrial claim construction orders are non-final by definition, as "the final determination of the construction of any claim ***occurs at the close of trial and manifests itself in the form of jury instructions***." *MediaTek Inc. v. Freescale Semiconductor, Inc.*, No. 11-CV-5341 YGR, 2014 WL 971765, at *2 (N.D. Cal. Mar. 5, 2014) (emphasis added). The Federal Circuit has recognized that a district court will often "revisit[] and alter[] its interpretation of the claim terms" as the case develops and the court's "understanding of the technology evolves." *Pressure Prods. Med. Supplies, Inc. v. Greatbatch, Ltd.*, 599 F.3d 1308, 1316 (Fed. Cir. 2010); *Conoco, Inc. v. Energy & Envtl. Int'l, L.C.*, 460 F.3d 1349, 1359 (Fed. Cir. 2006).[4]

Moreover, claim construction not only can but *must* be revisited when there is an intervening event, such as an IPR, that alters the intrinsic evidence. *See Lexington Luminance LLC v. Amazon.com Inc.*, 601 F. App'x 963, 970 n.5 (Fed. Cir. 2015) (instructing district court, on remand, "to determine whether the meanings of the disputed claim limitations have been altered by the [intervening] reexamination history" and explaining that "on remand, the district court may supplement its claim constructions consistent with the controlling appellate mandates as the case moves forward"); *Aylus Networks, Inc. v. Apple Inc.*, No. 13-CV-04700-EMC, 2016 WL 270387, at *5 (N.D. Cal. Jan. 21, 2016); *Evolutionary Intelligence, LLC v. Sprint Nextel Corp.*, 2014 WL 4802426, at *4 (N.D. Cal. Sept. 26, 2014) ("The IPR proceedings will also add

[4] *See also, e.g.*, *Kroy IP Holdings, LLC v. Autozone, Inc.*, No. 2:13-CV-888-WCB, 2015 WL 557123, at *2 (E.D. Tex. Feb. 10, 2015) ("[C]laim construction can be, and often is, an ongoing process that leads to refinements . . . .").

to the '536 Patent's prosecution history. Prosecution history is an important part of the intrinsic record relevant to claim construction."). Here, ACQIS not only altered the intrinsic record but, as discussed below, did so in a way that is irreconcilable with the prior court's constructions that ACQIS would still have this Court adopt.

B. Claims Must Be Construed in Light of the Teachings of the Patent Specification and the Prosecution History

The claim construction inquiry necessarily begins "by considering the language of the claims themselves." *Trustees of Columbia Univ. in City of N.Y. v. Symantec Corp.*, 811 F.3d 1359, 1362 (Fed. Cir. 2016). That is because the object of claim construction is "to understand and explain, ***but not to change***, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000) (emphasis added). Accordingly, the Federal Circuit frequently cautions against any construction that renders words in a claim meaningless or "mere surplusage" and requires that "claims are interpreted with an eye toward giving effect to all terms in the claim." *Texas Inst. Inc. v. U.S. Int'l Trade Comm'n*, 988 F.2d 1165, 1171 (Fed. Cir. 1993); *see also Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950–52 (Fed. Cir. 2006).

In determining the meaning of claim words, the Court does not work in a vacuum, but instead must use the specification as a guide to determine the terms' patent-specific meanings. As the Federal Circuit has recently reiterated, "[t]he ordinary meaning of a claim term is not 'the meaning of the term in the abstract,'" but rather "its meaning to the ordinary artisan after reading the entire patent." *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1320 (Fed. Cir. 2016). Accordingly, claim terms can and should be limited based on the overall teachings of the specification and the understanding conveyed to one of skill in the art by the embodiments disclosed. *See, e.g.*, *In re Abbott Diabetes Care Inc.*, 696 F.3d 1142, 1149 (Fed. Cir. 2012) (construing an "electrochemical sensor" to exclude external wires because "every embodiment

disclosed in the specification shows an electrochemical sensor without external cables or wires"); *Trustees of Columbia*, 811 F.3d at 1364.

Even where the claim language and specification would *not* in themselves compel a narrow construction, the Court must consider the prosecution history, which can alone preclude a broad construction. Indeed, the Federal Circuit has long held that when a patentee makes statements before the PTO to distinguish prior art from the claims, those statements are binding at claim construction, precluding broader constructions. For example, in *Springs Window Fashions L.P. v. Novo Industries, L.P.*, 323 F.3d 989 (Fed. Cir. 2003), the Federal Circuit held that the prosecution history required an additional limitation, not found expressly in the claims, because the patentee had argued that limitation was required in order to overcome a prior art rejection. *Id.* at 993–94. Accordingly, the patentee had disclaimed the broader scope that would otherwise have been permitted by the claims and specification. *See also, e.g.*, *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995) ("Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers."); *Gillespie v. Dywidag Sys. Int'l*, 501 F.3d 1285, 1291 (Fed. Cir. 2007) ("The patentee is held to what he declares during the prosecution of his patent."). Finally, even where a statement made during prosecution does not rise to the level of a binding "clear and unequivocal" disclaimer of claim scope, that statement may still provide compelling intrinsic record support that favors a narrower claim construction. *See, e.g.*, *NorthPeak Wireless, LLC v. 3com Corp.*, No. 2016-1477, 2016 WL 7448769, at *3 (Fed. Cir. Dec. 28, 2016); *Shire Dev., LLC v. Watson Pharm., Inc.*, 787 F.3d 1359, 1366 (Fed. Cir. 2015).

Post-issuance proceedings, including IPRs, are part of the prosecution history and can give rise to disclaimer or otherwise conclusively establish the meaning of a claim term. *See, e.g.*,

NorthPeak, 2016 WL 7448769, at *4 ("Even assuming the full scope of the plain meaning of 'register' were broader than that which we assign, we would, like the district court, find that NorthPeak unambiguously disclaimed a broader scope during reexamination."); *Pragmatus AV, LLC v. Yahoo! Inc.*, No. C-13-1176, 2014 WL 1922081, *5 (N.D. Cal. May 13, 2014) (holding that because "[u]nder Federal Circuit law, comments made by a patent holder during *inter partes* reexamination proceedings can limit claim scope," "[t]he same should be true now that *inter partes* review, rather than *inter partes* reexamination, is in effect.").

IV. "Peripheral Component Interconnect (PCI) Bus Transaction"

EMC Proposed Construction:	ACQIS Proposed Construction:
"a transaction, as defined in the industry standard PCI Local Bus Specification, involving a PCI bus"	"information, in accordance with the PCI standard, for communicating with an interconnected peripheral device"

Perhaps no issue better captures the extent to which ACQIS's proposals are contrary to the plain language of the claims and its own statements to the PTO than the term "PCI bus transaction." That term appears in every claim in this case, and is fundamental to the claimed inventions. EMC's construction is consistent with the plain language of the term and the disclosure in the specifications, as well as with ACQIS's own statements to the PTO in the IPRs.

EMC's proposed construction sets forth three requirements for a "PCI bus transaction." Specifically, a PCI bus transaction must be: (1) a transaction, (2) as defined in the industry standard PCI Local Bus Specification, (3) involving a PCI bus. The parties agree on the second requirement. Thus, the disputed issues are whether a "PCI bus transaction" must be a "transaction" (as opposed to mere "information"), and whether it must involve a "PCI bus."

Incredibly, as noted above, ACQIS has proposed a construction of the phrase "PCI bus transaction" that requires *neither* a "PCI bus" *nor* a "transaction." ACQIS's construction is irreconcilable with the clear, unambiguous language of the claims and the entirety of the

specification; its proposed construction also is precluded by ACQIS's statements in the IPRs.

A. A "PCI bus transaction" requires a transaction

In this case, the claim language itself is dispositive: a "PCI bus transaction" requires a "transaction." ACQIS attempts to eliminate that clear requirement by arguing that a PCI bus transaction should be defined broadly to require merely "information . . . for communication." While a "transaction" may involve information, it plainly is more than just information in the abstract; it is an active exchange of something (*e.g.*, an exchange of information) between two or more entities. By substituting the word "information" for the claimed "transaction," ACQIS improperly seeks to eviscerate the claims and erase the concept of a "transaction" from them entirely, even though they recite it explicitly. If ACQIS wanted to claim mere "information" sent in accordance with the PCI standard, ACQIS could have drafted its claims accordingly; ACQIS instead included the requirement of a "transaction," and ACQIS cannot remove that express requirement in the guise of seeking a construction. *See Embrex*, 216 F.3d at 1347; *Bicon*, 441 F.3d at 950–52.

ACQIS's effort to rewrite its claims—from requiring a transaction (as written) to merely requiring some information—must also be rejected, as a matter of black letter law, for a wholly independent reason: during the IPR, ACQIS represented to the PTO that a transaction (not just information) is actually required. In fact, ACQIS told the Board that it "should limit . . . 'PCI bus transaction' ***to a bus transaction*** according to [the] protocol standard." IPR '814 IPR Prelim. Resp. (Ex. 3) at 7 (emphasis added); ACQIS '873 IPR Prelim. Resp. (Ex. 2) at 6 (same).

ACQIS's argument to the PTO that "PCI bus transaction" actually requires a transaction is especially powerful because in an IPR, the Board is required to give the claims their "broadest reasonable construction." *See* 37 C.F.R. § 42.100(b). As the Federal Circuit has held, although "the broadest reasonable interpretation of a claim term may be the same as or broader than the

construction of a term" than a district court would enter in a litigation like this one, "***it cannot be narrower***." *Facebook, Inc. v. Pragmatus AV, LLC*, 582 F. App'x 864, 869 (Fed. Cir. 2014) (emphasis added). Stated differently, although a district court construction may properly impose *additional* limitations over and above the broadest reasonable construction, it cannot *remove* limitations; the construction in the PTO will by definition be the broadest reasonable one.

Here, ACQIS told the Board that even under the broadest reasonable construction, a "PCI bus transaction" requires a transaction, and not just information. ACQIS '814 IPR Prelim. Resp. (Ex. 3) at 6–10; ACQIS '873 IPR Prelim. Resp. (Ex. 2) at 5–8. The Board agreed, and adopted "Peripheral Component Interconnect (PCI) industry standard bus transaction" as its broadest reasonable construction of this term. '814 IPR Inst. (D.I. 126-3) at 7; '873 IPR Inst. (D.I. 126-2) at 7. ACQIS is now bound by its positions before the Board—which positions also are consistent with the plain language of the claims and uniform disclosure in the specifications. *See* ACQIS '814 IPR Prelim. Resp. (Ex. 3) at 6–9 (citing '814 patent at 19:31–39). ACQIS nevertheless relies on, and urges this Court to adopt, an older, broader construction from Judge Davis. That construction not only is inconsistent with the plain language of the claims—requiring a transaction, not merely information—but also with ACQIS's statements to the PTO *after* Judge Davis adopted his construction, statements ACQIS made to save its patents.

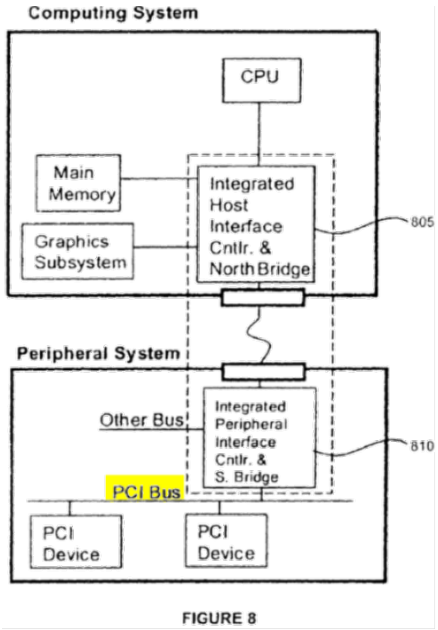
The term "PCI bus transaction" requires a transaction—that is what the plain language means and specifications disclose, and that is exactly what ACQIS told the PTO in the IPRs.

B. A "PCI bus transaction" requires a PCI bus

The intrinsic evidence, beginning with the claims themselves, also uniformly confirms that the claims require a transaction involving an actual "PCI bus." Indeed, the very notion that a PCI bus transaction need not involve a PCI bus (as ACQIS contends) is absurd, and finds not a shred of support anywhere in the intrinsic record. The claims recite a "*PCI bus* transaction"—

not just any generic transaction involving an "interconnected peripheral device." And ACQIS agrees that the term "PCI bus" refers not to any generic bus but to the "industry standard computer bus known as the Peripheral Component Interconnect Local Bus." D.I. 71 at 32. While ACQIS could have attempted to secure the claims in the broader way it now advocates, it did not. The claims themselves mandate that a "PCI bus transaction" requires at least one PCI bus to be involved in the transaction.

In addition, the specifications of the asserted patents uniformly disclose PCI bus transactions as involving at least one PCI bus (and, in most cases, occurring between two PCI buses). For instance, the specifications refer to "a general, industry-standard PCI bus controller," and explain that "PCI bus[es] are well known and understood in the industry." '873 patent at 24:31–35, 25:42–45, 31:8–9; '814 patent at 13:48–52, 14:56–60, 18:4–6. Every single embodiment described in the patents involves a PCI bus, and every single figure depicting the interface architecture includes a PCI bus. The one figure that does not expressly depict a PCI bus on the CPU side ('873 patent, Fig. 8; '814 patent, Fig. 18; '468 patent, Fig. 18), clearly shows a PCI bus on the peripheral side:



Simply put, there is no disclosure—in any of the specifications of the asserted patents—of a PCI bus transaction that does not involve a PCI bus. Where, as here, "nothing suggests or even hints" that the claimed invention need not involve a PCI bus, a construction of "PCI bus transaction" that does not require a PCI bus is in error. *In re Abbott*, 696 F.3d at 1150.[5]

That the claimed "PCI bus transaction" must involve a PCI bus also follows from the fundamental purpose of the invention: to allow the use of consoles and modules containing existing industry standard PCI buses, but to improve the interface channel over which they communicate. As the specifications explain, "the prior art interface include[d] a very large number of signal channels with a corresponding large number of conductive lines," which had the disadvantages of being more expensive, "bulkier and more cumbersome to handle," and slower. '873 patent at 3:49–67. The claimed inventions were aimed at solving these problems: "the interface channel, XPBus, of the present invention uses fewer lines than are contained in either of the buses which it interfaces, namely the PCI buses." '873 patent at 18:45–47; ACQIS '873 IPR Prelim. Resp. (Ex. 2) at 8 ("[O]ne of the goals of the invention is to serialize PCI protocol standard signals specifically, not some generic signal or alternative . . . ."); IPR Hr'g Tr. (Ex. 13) at 40:21–25 ("[T]he claim is actually to ***solve a specific problem with systems using PCI***.") (emphasis added). If no PCI bus were involved at any point, it would defeat the entire purpose of the invention. A construction so dissonant with the purpose of the invention cannot be correct. *Honeywell Int'l, Inc. v. United States*, 609 F.3d 1292, 1299 (Fed. Cir. 2010)

[5] Notably, EMC's current proposed construction eliminates one of Judge Davis's concerns with EMC's prior proposed construction. Judge Davis objected to EMC's prior construction because, as seen in Figure 8, "information in accordance with the PCI standard can be encoded and conveyed serially without the existence of an *originating* PCI bus." D.I. 71 at 10 (emphasis added). EMC's current proposed construction does not mandate the existence of an *originating* PCI bus, but would allow the PCI bus to be involved at any point in the transaction.

(affirming a construction of "local color display" that required color bands visible to the human eye because the fundamental purpose of the invention was to convey warning signals).

Consistent with the claims and the written description all requiring a PCI bus, the prosecution histories of the asserted patents also confirm that both ACQIS and the PTO understood the claimed "PCI bus transaction" to be a transaction requiring the presence of at least one PCI bus. In reexamining the related '779 patent, for example, the Board explained that "[o]ne of ordinary skill in the art also would have understood that ***a PCI bus would be used*** to transmit (or communicate) data pertaining to PCI bus transactions." '779 Reexam, Decision on Appeal (Ex. 18) at 8 (emphasis added). Likewise, in the reexamination of the related '185 patent, ACQIS distinguished prior art precisely because it did *not* disclose a PCI bus. '185 Reexam, Resp. to OA (Ex. 17) at 11 ("Rather than disclosing a PCI bus, McNamara refers to 'an ISA bus or an EISA bus,' which is different from a PCI bus."). These statements further confirm what is already clear from the claim language: a "PCI bus transaction" must involve an actual PCI bus at some point in the communication process. *Springs Window Fashions*, 323 F.3d at 994; *NorthPeak*, 2016 WL 7448769, at *3.

Finally, during the IPRs, ACQIS confirmed that a PCI bus is required in a PCI bus transaction, and in fact distinguished prior art on exactly this basis. Specifically, ACQIS contended that the prior art (Horst and Bogaerts) did not have a PCI bus transaction in the module because there was no PCI bus: "Figure A [of Horst] illustrates that in the upper portion of Horst, which is the CPU side [*i.e.*, module], there is no PCI bus. And, ***consequently***, the TNet link does not generate PCI bus transactions or PCI transactions at the CPU side. Bogaerts similarly removes the PCI bus." '814 PO Resp. at 4 (emphasis added); *see also id.* at 20. Thus, by arguing that there was no PCI bus transaction without involving a PCI bus, ACQIS confirmed

that a PCI bus is required for a PCI bus transaction.[6]

Similarly, the Board recognized that ACQIS's fundamental invention was directed to "interfacing two Peripheral Component Interconnect ('PCI') ***buses***" by "encoding a PCI industry standard bus ***transaction*** so that it can be communicated on a serial connector." '814 IPR Decision (D.I. 126-5) at 4, 10 (emphases added); '873 IPR Decision (D.I. 126-4) at 9–10 (same). The Board recognized, just as ACQIS argued and the PTO had previously found, that a PCI bus transaction involves a PCI bus.

In short, the claims, the specification, and the prosecution history (including the IPRs) all confirm that the correct construction of "PCI bus transaction" is "a transaction, as defined in the industry standard PCI Local Bus Specification, involving a PCI bus."

V. "Encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction" and related terms

Exemplary Claim Language:	
"encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction" ('873 patent, cls. 6, 54 & 65) "serial channels that transmit encoded data of Peripheral Component Interconnect (PCI) bus transaction" ('814 patent, cl. 24) "an encoded serial bit stream . . . of [a] Peripheral Component Interconnect ("PCI") bus transaction" ('468 patent, cl. 29)	
EMC Proposed Construction:	**ACQIS Proposed Construction:**
"a PCI bus transaction that has been serialized from its original parallel format"	Plain and ordinary meaning

All of the asserted claims contain phrases that, in various forms, recite that data of a "PCI

[6] Unlike in the instant litigation, the issue of whether a PCI bus was required was not disputed when the Board entered its broadest reasonable construction of "PCI bus transaction." Although ACQIS, at oral argument in the IPR, later made self-serving statements that "the claims don't require a bus" (*see* IPR Hr'g Tr. (Ex. 13) at 46:14–47:18), those statements were not adopted, and are not entitled to weight on claim construction. *See, e.g.*, *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1270 (Fed. Cir. 1986) ("self-serving statements" made in post-issuance prosecution "likely would be accorded no more weight than testimony of an interested witness or argument of counsel" in determining claim construction).

bus transaction" has been "serialized," transmitted in "serial form" or transmitted over "serial bit channels." The language of claims, the uniform teaching of the specifications, and ACQIS's repeated statements before the PTO all compel that these phrases should be construed to require that the PCI bus transaction has been "serialized from its original parallel format." And, this is exactly how ACQIS has described the claimed inventions: "one key to the invention was to serialize the otherwise parallel PCI bus transactions." ACQIS '814 IPR Resp. (Ex. 5) at 3.

Despite the plain claim language and its own statements regarding its own patented inventions, ACQIS now contends—again, without a shred of support in the intrinsic record—that the claims do not really require that the PCI bus transaction be serialized from its original parallel format. ACQIS wrongly asserts that even a signal that was entirely serial from the outset, and thus never "serialized" from an original parallel format, could somehow satisfy the claims. ACQIS's effort to rewrite its claims in order to broaden them for infringement purposes ignores not just the claim language, but every single disclosed embodiment of the specification, as well as ACQIS's own assertions during the IPRs that converting from parallel to serial is a critical aspect of the invention that ACQIS used to differentiate the claims from the prior art.

The language of the claims on its own compels EMC's construction. The phrases at issue fall into two groups: (1) those claims that recite that the PCI bus transaction data is in serial form (or in a "serial bit stream," or as "serial data") and (2) those claims that recite that the PCI bus transaction data is transmitted over a serial channel. *See* Appendix B. There is no dispute that, as previously discussed, a PCI bus transaction, when it is generated, is necessarily in parallel format. *See supra* Section II. Accordingly, with respect to the first group of claims, because they expressly cite that this originally parallel data must be sent in serial form, that necessarily requires that the data was "serialized," *i.e.*, converted from serial to parallel. Similarly, with

respect to the second group of claims, because they require that this originally parallel PCI data is sent over a serial line, that too inherently requires that the data is serialized, as parallel data would not fit down the fewer lines in a serial connector. *See* Young '814 IPR Decl. (Ex. 1) ¶¶ 25–28. In sum, in all instances, the claim language alone necessarily requires the parallel to serial conversion embodied by EMC's proposed construction.

The specification confirms EMC's construction. The specification explains that the parallel data will be converted to serial form so that it may be sent over the serial connector. And, every single disclosed embodiment depicts a serialization of originally parallel PCI bus transaction data—which, as the Federal Circuit has held, is strong evidence that the claims should be construed accordingly. *See, e.g.*, *In re Abbott*, 696 F.3d at 1149. Specifically, Figures 7 and 8 of the '873 patent, which are found in all asserted patents (expressly or through incorporation), disclose two embodiments of the invention whereby PCI bus transaction data is transferred between a console (labeled "peripheral system") and a module (labeled "computing system") over a serial channel (the curved line connecting the two):

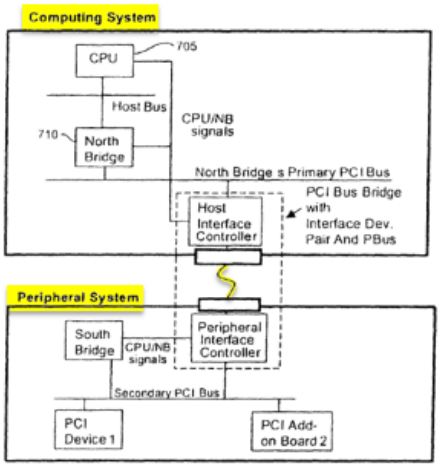


FIGURE 7

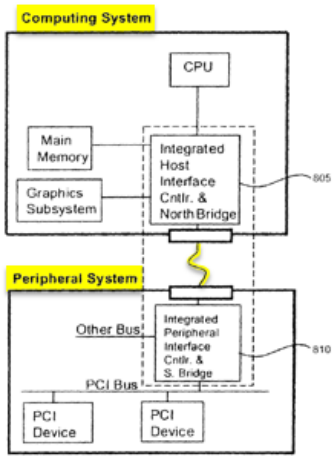


FIGURE 8

See '873 patent at Figs. 7 & 8, 15:21–30; *see also* '814 patent at Figs. 11 & 18, 20:7–29, 25:44–51; '468 patent at Figs. 13, 17, 18 & 20, 18:34–19:8.

In both embodiments, parallel data is converted to serial data, transferred over the serial

line, and then converted back to parallel by "interface controllers" that are shown at the boundaries. Figure 10, which details the architecture of the "interface controllers" of Figures 7 and 8, also makes this point clear, in that all inbound data entering the controller (from right to left) goes into a "serial to parallel converter," whereas all outbound PCI bus transaction data leaving the controller (from left to right) goes through a "parallel to serial converter":

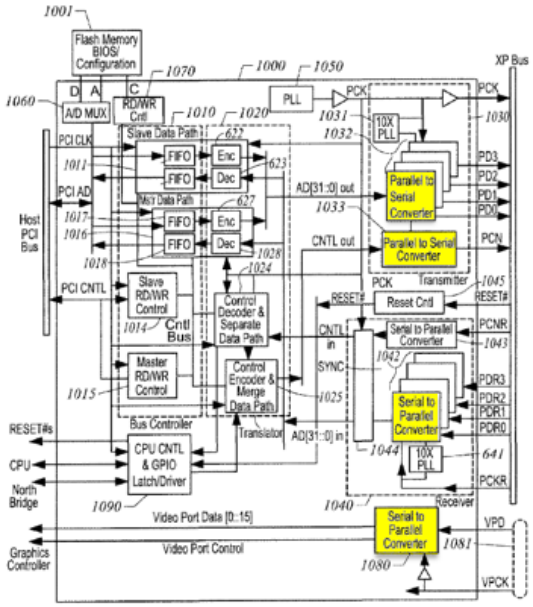


FIGURE 10

See '873 patent at Fig. 10, 17:54–60, 18:16–23; *see also* '814 patent at Figs. 12A & 12B, 21:54–22:3; '468 patent at Fig. 14, 19:47–53. All of the PCI bus transaction data goes through a "parallel to serial converter" or a "serial to parallel converter" precisely because the parallel PCI data is serialized for transmission and then converted back to parallel when it arrives.

There is simply no disclosure, anywhere in the patents, of sending PCI bus transaction data in serial form without first "serializing it" (*i.e.*, converting it) from its original parallel form; nor could there be, considering a PCI bus transaction, when it is generated, is necessarily in parallel format and must be serialized to use a serial connector, as required by the claims.

Finally, ACQIS's litigation position here is totally inconsistent with the arguments it made in an effort to avoid having its patents invalidated over the prior art during the IPRs. In

those proceedings, ACQIS repeatedly and unequivocally stated that "serialization," or conversion from parallel-to-serial, is a *required* aspect of the claims. As the Federal Circuit has long held, when an applicant for a patent makes clear and unequivocal statements to distinguish the claims from the prior art, those arguments are binding and limit the scope of the claims for claim construction. *See Springs Window Fashions*, 323 F.3d at 994. Here, ACQIS could not have been more clear.

At the final IPR hearing before the Board, for example, ACQIS emphasized to the Board that the entire invention centered on serialization of parallel PCI:

> But the whole point of this invention and these claims is that they are centered around dealing with a standard. All of the computers out there have PCI. . . . ***And the point is you take it from parallel to serial and then back to parallel.***

IPR Hr'g Tr. (Ex. 13) at 34:14–18 (emphasis added). ACQIS's clear and binding statement—*i.e.*, that the claims require serializing data that was in parallel form and then taking it back to parallel form at the other end—which was made in an effort to distinguish and overcome the prior art, alone confirms and compels EMC's construction.

Nor was that statement an isolated comment. To the contrary, ACQIS represented that the claims *require* serializing a parallel PCI bus transaction at numerous other points during the IPRs. Indeed, ACQIS's own expert agreed that "the claims . . . contemplate some sort of transformation of the PCI bus transaction into a format that is serially transmitted and then, on the other end, it would be converted back into PCI bus transaction format." Lindenstruth Dep. Tr. (Ex. 9) at 149:20–150:5. ACQIS's expert further explained that the patents "are basically serializing the particular ongoing PCI transaction which is being then made parallel on the far end again." *Id.* at 190:23–191:1.

In fact, in its IPR papers, ACQIS explicitly represented that "one key to the invention was to serialize the otherwise parallel PCI bus transactions." ACQIS '814 IPR Resp. (Ex. 5)

at 3. ACQIS then distinguished several prior art references (*e.g.*, Horst and Bogaerts) precisely because they did *not* perform this critical serialization step. *Id.* at 24 (distinguishing the prior art because "Horst never serializes any PCI bus transaction"); *id.* at 39 (Horst "never serializes an actual PCI bus transaction as required for claim 31."); *id.* at 43 (Bogaerts "never serializes an actual PCI bus transaction."); ACQIS '873 IPR Resp. (Ex. 4) at 1, 3, 21–22 (same).

ACQIS also repeatedly argued that the claims require serializing a parallel PCI bus transaction at the hearing. Describing the claimed invention, for example, ACQIS stated: "You start with the PCI address that's in this parallel slow form, serialize it and then take it back to the PCI form at the other end." IPR Hr'g Tr. (Ex. 13) at 32:2–4. ACQIS reiterated this exact point several times, explaining, for example: "So I have created my PCI transaction. . . . And then I'm taking it at a parallel form, putting it into serial form and then back to parallel." *Id.* at 46:14–47:18. So fundamental to the patents is the conversion of parallel to serial that ACQIS repeatedly represented that it is a requirement of the claims. Every one of these many unequivocal statements is binding as a matter of law, and each one alone is sufficient to compel EMC's construction.[7]

ACQIS does not deny making these binding statements, of course. Rather, ACQIS simply ignores them, and contends only that the claims should not be construed as EMC proposes because Judge Davis reached a different conclusion regarding the "encoded" phrases.[8]

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[7] The language of the claims before the PTO is comparable to the other claims at issue. *See* Appendix A. The Federal Circuit has repeatedly held that disclaimers made in one patent apply to related patents containing the same or similar terms. *Trading Techs. Int'l, Inc. v. Open E Cry, LLC*, 728 F.3d 1309, 1323 (Fed. Cir. 2013) ("prosecution history regarding a particular limitation in one patent is presumed to inform the later use of that same limitation in related patents").

[8] ACQIS incorrectly claims that EMC's proposal ignores the agreed construction of "serial bit stream." ACQIS CC Stmt. (Ex. 21) at 2–3. EMC does not propose that this agreed construction, which is entirely consistent with EMC's current proposal, be altered.

That argument ignores the obvious and dispositive fact that Judge Davis did not have ACQIS's clear and binding disclaimers from the IPRs. Indeed, at the time Judge Davis considered the issue, ACQIS had never clearly stated that serialization was a required aspect of the claims. ACQIS made that representation in the IPRs when it considered it necessary to do so to differentiate the prior art in order to save its patents. Having done so—and having obtained the benefit of doing so by defeating the IPRs—ACQIS is bound (and the claims are limited) by those statements. Those representations (*i.e.*, that the claims require the parallel data to be serialized) also are consistent with the totality of the intrinsic record, including the claims themselves—all of which compel EMC's construction.

VI. "Communicating . . . PCI bus transaction" and related terms

Exemplary Claim Language:	
"communicating . . . Peripheral Component Interconnect (PCI) bus transaction" ('873 patent, cls. 54 & 65) "communicate address and data bits of PCI bus transaction" ('814 patent, cls. 24 & 31) "transmit . . . Peripheral Component Interconnect ("PCI") bus transaction address and data" ('119 patent, cl. 38)	
EMC Proposed Construction:	**ACQIS Proposed Construction:**
"communicating a PCI bus transaction, including all address, data, and control bits, without discarding any of those bits"	Plain and ordinary meaning

In addition to generating and serializing a PCI bus transaction, the claims require "communicating" or "transmitting" that PCI bus transaction within the system. *See* Appendix B (identifying the various forms of this limitation in the asserted claims). But it is not enough to communicate *some*—or even *most*—bits of a PCI bus transaction. Rather, as Judge Davis explained in the prior *Markman* order, "a PCI bus transaction must include *all* information required by the PCI standard." D.I. 71 at 10 (emphasis added).

ACQIS also has repeatedly and unambiguously represented (again, in distinguishing prior

art to survive the IPRs) that the claims require communicating *all* (not just some) bits of a PCI bus transaction required under the PCI Local Bus Specification. The PCI standard requires, *inter alia*, address bits (which specify the location of the data requested or where data is being sent), data bits (which are the data requested or the data to be stored), and control bits (which control the timing of events on the PCI bus). *See, e.g.*, PCI standard (Ex. 14) at 7–11, 25–26, 35–37; *see also* IPR Hr'g Tr. (Ex. 13) at 35:11–17, 50:12–16. ACQIS has maintained that for a PCI bus transaction, *all* of these bits are required. *See id.* at 31:18–32:4, 35:13–17, 38:9–12. And, as explained below, ACQIS distinguished the prior art in the IPRs for not communicating all address, data, and control bits, and for discarding bits of the PCI bus transaction during communication. As ACQIS's counsel succinctly put it, referring to the address, data, and control bits of a PCI bus transaction: "[Y]ou got to have them all." IPR Hr'g Tr. (Ex. 13) at 49:12–16; *id.* at 35:13–17, 38:9–12.

Now, in this litigation, having survived the IPRs, ACQIS accuses technology that does *not* communicate all bits required by the parallel PCI standard. Hence, despite its unambiguous statements in the IPRs, ACQIS now contends that it is not really necessary to send all bits. That is, while in the IPRs, ACQIS said about the bits of a PCI bus transaction, "you got to have them all," here to prove infringement, ACQIS now essentially claims "you ***don't*** got to have them all." ACQIS cannot undo its clear statements during the IPRs to keep its infringement case alive: the claims require "communicating a PCI bus transaction, including all address, data, and control bits, without discarding any of those bits," just as ACQIS said they do during the IPRs.

In fact, in the IPRs, ACQIS argued that *all* bits were required *in response* to EMC's position that the plain language of the challenged claims, under their broadest reasonable interpretation, could be read to allow for transfer of fewer than all bits of PCI bus transaction.

EMC '814 IPR Reply (Ex. 8) at 3, 5; *see also* EMC '873 IPR Reply (Ex. 7) at 3, 5. ACQIS vehemently disagreed with EMC's interpretation of the claims, and emphasized the importance of "adher[ing] to the PCI standard." ACQIS '814 IPR Resp. (Ex. 5) at 8–9; *see also* ACQIS '873 IPR Resp. (Ex. 4) at 8. ACQIS explained that adhering to the PCI standard *requires* communicating *all* address, data, and control bits, and not communicating all required bits would "make sure [the transaction] does not comply with either the standard of a PCI or the purpose of the invention." *See* IPR Hr'g Tr. (Ex. 13) at 35:11–17; 38:15–17; *id.* at 38:5–12 (ACQIS emphasizing that claims require communicating "the information necessary to make a PCI transaction under the defined standard," which "includes the control bits every time").

ACQIS then distinguished the prior art for failing to communicate *all* required address, data, and control bits. For example, with respect to communicating the required address bits, ACQIS distinguished Horst because "use of the TNet protocol means that PCI address bits are not transmitted over the TNet links." ACQIS '814 IPR Resp. (Ex. 5) at 24; *see also* ACQIS '873 IPR Resp. (Ex. 4) at 22 (same). It was ACQIS's position that, even if 12 of the 32 address bits are communicated with the TNet protocol in Horst, Horst did not communicate *all* bits and thus did not communicate a PCI bus transaction. S*ee id.* at 24, 27–29; *see also* ACQIS '814 IPR Surreply (Ex. 11) at 2; ACQIS '873 IPR Surreply (Ex. 12) at 2–3. In the '814 IPR, ACQIS distinguished Bogaerts on similar grounds. *See* ACQIS '814 IPR Resp. (Ex. 5) at 42–45.

ACQIS similarly distinguished both key prior art references at issue for not disclosing communication of control bits:

> So you didn't hear a word about control bits, period. There is no such thing – just put it bluntly, ***there is no such thing as a PCI bus transaction that does not have control bits. To carve control bits out of claim 54 and 61 is to make sure it does not comply with either the standard of a PCI or the purpose of the invention***. So when we talk about 54, you have to talk about control bits. ***And not once do they talk about Horst or Bogaerts transmitting any type of control bits***. Just doesn't happen.

Id. at 38:12–20 (emphases added). ACQIS's expert reiterated that the claims require communicating control bits:

> ***Q: Does that mean that all of the elements of the PCI bus transaction have to be encoded, including the address, data, control signals, et cetera?***
>
> ***A. Whatever pertains to the PCI transaction otherwise it wouldn't be complete, yeah.***

Lindenstruth Dep. Tr. (Ex. 9) at 168:17–169:8 (emphasis added). He further testified that *all* bits are "part of what the claims require as a PCI bus transaction." *Id.* at 145:18–146:17.

ACQIS also distinguished the prior art because it "discards" some bits of a PCI bus transaction. *See* ACQIS '814 IPR Resp. (Ex. 5) at 43–45; *see also* ACQIS '814 IPR Surreply (Ex. 11) at 2–3. For example, although Bogaerts disclosed a PCI bus transaction in the module, ACQIS argued that when the PCI bus transaction is received by an adapter, the system "discards . . . a portion of the PCI address . . . required for a PCI bus transaction," and for *that reason* (*i.e.*, because it discards some address bits) it does not disclose "communicat[ing] said address and data bits of PCI bus transaction." *See* ACQIS '814 IPR Resp. (Ex. 5) at 43–45; *see also* ACQIS '814 IPR Surreply (Ex. 11) at 2–3; Lindenstruth Dep. Tr. (Ex. 10) at 322:14–323:21.

ACQIS's disclaimer—*i.e.*, that the claims require communicating *all* bits of a PCI bus transaction required under the PCI standard—is entirely consistent with the specifications of the asserted patents, which uniformly depict serializing and communicating *all* bits of a PCI bus transaction, including the address, data, and control bits.[9] There is not a single embodiment in any of the patents that shows communicating a PCI bus transaction without communicating the

[9] For example, Figure 10 of the '873 patent (which is in all the patents) is a detailed block diagram of "the host interface controller ['HIC'] of the present invention." '873 patent at 8:4–5, 16:23–24. As seen in the left of the figure, the HIC is coupled to a "Host PCI Bus." The HIC receives both the PCI address and data (on the "PCI AD" line) and the PCI control (on the "PCI CNTL" line). *See id.* All of these signals (address, data, and control) are encoded and serialized to be sent over the XPBus. *Id.* at 16:38–17:40; *see also* '814 patent at 20:30–22:3.

address, data, and control bits. Rather, *every single embodiment* discloses communicating *all* the address, data, and control bits—which is strong evidence that the claims should be construed accordingly. *See In re Abbott*, 696 F.3d at 1149.

ACQIS's criticism of EMC's proposal ignores the IPR record and the law. ACQIS suggests that, because some of the claims have language modifying the phrase "PCI bus transaction" (*e.g.*, "*address and data bits* of PCI bus transaction," "*data* of PCI bus transaction," and "PCI bus transaction *address and data*"), fewer than all the bits of an entire PCI bus transaction could be conveyed. *See* ACQIS CC Stmt. (Ex. 21) at 2. But that is the exact argument that EMC made during the IPRs, and that ACQIS argued against and the PTO rejected. ACQIS's effort to advance an argument here that it rebutted in the IPRs and the PTO rejected is disingenuous. In any event, by virtue of its arguments to overcome prior art, ACQIS has forever surrendered the broad claim scope it now seeks. *Springs Window Fashions*, 323 F.3d at 993.[10]

Consistent with ACQIS's statements, communicating a PCI bus transaction requires communicating *all* address, data, and control bits of a PCI bus transaction.

VII. Conclusion

For the foregoing reasons, EMC respectfully requests that this Court adopt EMC's proposed claim constructions for the three terms at issue here. Although EMC has not addressed additional claim construction issues here, EMC maintains its objections to Judge Davis's constructions, and reserves its right to address additional terms in the future in this case.

[10] Indeed, the modifying language that ACQIS points to as evidence that one could communicate fewer than "all bits" was also present, in the same or similar form, in the very claims ACQIS distinguished from the prior art during in the IPRs. *See, e.g.*, '873 patent, cl. 61; '814 patent, cl. 24. When ACQIS argued that those claims still require communicating not just address and data bits, but *all* required bits, including all control bits, ACQIS relinquished any contrary argument.

Date: January 20, 2017

Respectfully submitted,

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LOCAL RULE 7.1(A)(2) CERTIFICATION

Pursuant to Local Rule 7.1(a)(2), undersigned counsel hereby certifies that EMC conferred with counsel for the Plaintiff ACQIS, LLC in a good faith attempt to resolve and/or narrow the issues addressed in this motion. ACQIS has advised that it does not oppose this motion.

/s/ John A. Gallagher
John A. Gallagher

CERTIFICATE OF SERVICE

I, John A. Gallagher, hereby certify that on this 20th day of January 2017, I caused true and accurate copies of the within document to be served on all counsel who have requested notice in this case via the Court's CM/ECF system.

/s/ John A. Gallagher
John A. Gallagher